

WINTERLOGIC PARTNERS WITH ICON DESIGN AUTOMATION FOR SALES AND DISTRIBUTION IN INDIA

Roseville, MN – October 15, 2008 – WinterLogic Inc., a leading supplier of Verilog fault simulation tools, today announced that it has expanded its sales efforts to India with an exclusive distribution agreement with ICON Design Automation of India.

“As India continues to grow in importance as an EDA design community, we are excited to have ICON working with us to provide customers in India direct sales and support. Because they have offices throughout India as well as provide a strong team of sales and support engineers, we will be well-positioned in this market.” stated Jason Campbell, president of WinterLogic.

“WinterLogic’s functional fault simulation tools are gaining a reputation for significant reduction of test development time for electronic designs,” remarked R Varalakshmi, CEO of ICON. “We are delighted to be associated with this leading-edge, industry-proven product for the Indian market.”

About Z01X Fault Simulator

Based on WinterLogic’s proprietary C2 algorithm, Z01X is the fastest functional fault simulator available. Z01X is also the only Verilog fault simulator that has the capability of simulating stuck-at, transition and bridge faults. Z01X supports the full Verilog IEEE 1364-2001 language and accepts WGL, STIL, VCD or testbench stimulus.

About ICON Design Automation

ICON Design Automation handles leading chip design tool companies for the India market through its offices at Bangalore, Hyderabad and New Delhi, headquartered at No. 3016, 5th Cross, 12th ‘B’ Main, HAL 2nd Stage, Bangalore - 560008. For more information, visit www.icon-dapl.com.

About WinterLogic

Established in 2005, WinterLogic specializes in helping companies achieve their DPM targets and reduce tester time. We have special expertise in high-speed fault simulators and fault management environments for Verilog designs. Our unique technologies dramatically improve the performance of fault simulation. Our proprietary expert test system uses “testability analysis” to provide optimum test ordering, eliminate redundant tests and report on uncovered areas of the design before fault simulation begins. For more information, visit www.winterlogic.com.

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